

<b>Notice of References Cited</b>	Application/Control No. 09/580,854	Applicant(s)/Patent Under Reexamination SIRICHOTIYAKUL ET AL.	
	Examiner Kandasamy Thangavelu	Art Unit 2123	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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	B	US-5,751,593	05-1998	Pullela et al.	716/6
	C	US-6,175,949	01-2001	Gristede et al.	716/11
	D	US-6,097,241	08-2000	Bertin et al.	327/534
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	H	US-5,831,451	11-1998	Bosshart	326/93
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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Sundararajan et al., "Low power synthesis of dual threshold voltage CMOS VLSI circuits", ACM 1999
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

